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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,462	07/07/2003	Tzu-Chiang Sung	252011-1490	7583

24504 7590 09/15/2004

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EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,462	SUNG ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "overlay of the gate and the second well is defined as zero" must be shown or the feature(s) canceled from the claim(s). Note that Figures 4 and 5 clearly show the gate overlying both the first and second wells and therefore the overlay is not zero. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1, 9, 15, and 23 are objected to because of the following informalities:

In regards to claim 1, the limitation "of the first" in line 3 of the claim should be changed to "of the first type". Furthermore, the limitation "a first and second well" should be changed to either "a first well and a second well" or "[[a]] first and second wells". This also applies to the limitation "a first and second doped region". Claim 15 has similar problems.

In regards to claim 9, the limitation "a first P and N well" is objected to for being unclear. It is suggested this limitation be changed to either "a first P well and a first N well" or "[[a]] first P and N wells". This also applies to the limitation "a second N and P well". Claim 23 has similar problems.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 7, 15, 17, 19, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu et al. (US Pat. 6,265,752, hereinafter Liu).

In regards to claims 1, 7, 15, and 21, Figure 5 of Liu discloses a high voltage device comprising a substrate 20 of a first type (p-type); first and second wells (P-well and N-well) respectively of the first type and a second type (n-type) in the substrate; a gate 30/28 formed on the substrate; a first doped region (n-region in P-well) and a second doped region 32 both of the second type, respectively formed in the first and second well and both sides of the gate; and a third doped region (p-region in P-well) of the first type in the first well and adjacent to the first doped region. In regards to claim 15, the device of Liu must be made by the claimed method.

In regards to claims 3 and 17, Figure 5 of Liu discloses the gate 30/28 comprises a gate oxide 28 on the substrate 20, a conducting layer 30 on the gate oxide and spacers 34 on two sides of the gate oxide and conducting layer.

In regards to claims 5 and 19, Figure 5 discloses there is a spacing of the second doped region (n-region in P-well) to the gate 30/28.

Claims 1, 2, 5-10, 13-16, 19-24, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Ito et al. (US Pat. 5,856,695, hereinafter Ito).

In regards to claims 1, 7, 15, and 21, Figures 3-23 of Ito disclose a high voltage device comprising: a substrate of a first type (p-type); first and second wells (850 and 750, respectively, see Figure 8) respectively of the first type and a second type (n-type) in the substrate; a gate 1350 (Figure 13) formed on the substrate; a first doped region 1550 (Figure 15) and a second doped region 1556 both of the second type, respectively formed in the first and second well and both sides of the gate; and a third doped region 1850 (Figure 18) of the first type in the first well and

adjacent to the first doped region. In regards to claim 15, Figures 3-23 of Ito also disclose the method of making the claimed device.

In regards to claims 2 and 16, Figure 6 of Ito discloses field oxides (610 and 620) isolating the high voltage device from other devices (TFR resistor) on the substrate.

In regards to claims 5 and 19, Figures 3-23 of Ito discloses there is a spacing of the second doped region 1556 to the gate 1350.

In regards to claims 6 and 20, Figure 18 of Ito discloses the overlay of the gate 1350 and the second well 750 is defined as zero.

In regards to claims 8 and 22, Ito discloses the conductivity types can be reversed (col. 19, lines 28 and 29). Therefore, the first type will be n-type and the second type will be p-type. Figure 8 of Ito disclose buried layer 450 (now N+) in the substrate and beneath the first and second well (850 and 750).

In regards to claims 9 and 23, Figures 3-23 of Ito disclose a high voltage device formed on a P substrate comprising: an HVNMOS comprising: a first P and N well (850 and 750, respectively, see Figure 8) in the P substrate; a first gate 1356 (Figure 13) formed on the P substrate; two first N+ doped regions (1550 and 1556, Figure 15) respectively formed in the first P and N well, and both sides of the first gate; and a first P+ doped region 1850 (Figure 18) in the first P well and adjacent to the first N+ doped region in the first P well; and a HVPMOS comprising: an N+ buried layer 370 (Figure 8) in the substrate; a second N and P well (770 and 860, respectively, see Figure 8) in the P substrate and above the N+ buried layer; a second gate 1160 (Figure 13) formed on the P-substrate; two second P+ doped regions (1870 and 1860, Figure 18) respectively formed in the second N and P well, and both sides of the second gate;

and a second N+ doped region 1570 (Figure 18) in the second N-well and adjacent to the second P+ doped region in the second N well. In regards to claim 23, Figures 3-23 of Ito also disclose the method for making the claimed device. Note that the limitations "high voltage" or "HV" are merely functional/intended use limitations that do not structurally distinguish the claimed invention over the prior art. The MOS devices of Ito are capable of operating under a high voltage condition. It should also be noted that "high voltage" is a relative term and any voltage (other than 0 volts) can be considered a "high" voltage.

In regards to claims 10 and 24, Figure 6 of Ito discloses field oxides (610 and 620) isolating the high voltage devices from other devices (TFR resistor) on the substrate.

In regards to claims 13 and 27, Figures 18 of Ito disclose there is a spacing of the first N+ doped region 1556 in the first N well 750 to the first gate 1350 and the second P+ doped region 1860 in the second P well 860 to the second gate 1160.

In regards to claims 14 and 28, Figure 18 of Ito discloses the overlay of the first gate 1356 and the first P well 850 and the second gate 1160 and the second N well 770 are defined as zero.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 11, 13, 23, 25, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Wei (US Pat. 6,403,992).

In regards to claims 9 and 23, Figure 5 of Liu discloses a high voltage device formed on a P substrate 20 comprising: an HVNMOS comprising: a first P and N well, in the P substrate; a first gate 30/28 formed on the P substrate; two first N+ doped regions (32 and n-region in P-well) respectively formed in the first P and N well, and both sides of the first gate; and a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well. Liu also discloses an N+ buried layer 22 beneath the wells. Note that Liu also discloses the method of making the device. The difference between Liu and the claimed invention is having a complimentary HVPMOS of the same structure on the substrate. Figure 2 of Wei discloses an HVNMOS and an HVPMOS on a P-substrate. The HVNMOS and the HVPMOS of Wei have the same structure except that the conductivity types are reversed. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Liu by including an HVPMOS on the substrate, wherein the HVPMOS has the same structure as the HVNMOS. The ordinary artisan would have been motivated to modify Liu in the manner described above for the purpose creating a CMOS device, thereby increasing switching speed and increasing noise immunity, which is well known in the art.

In regards to claims 11 and 25, Figure 5 of Liu discloses the gate 30/28 comprises a gate oxide 28 on the substrate 20, a conducting layer 30 on the gate oxide and spacers 34 on two sides of the gate oxide and conducting layer.

In regards to claims 13 and 27, Figure 5 of Liu discloses all the doped regions are spaced from the gate 30/28.

Claims 3, 4, 11, 12, 17, 18, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito in view of McElheny et al. (US Pat. 6,740,944, hereinafter McElheny).

In regards to claims 3, 4, 17 and 18, Figure 13 of Ito discloses the gate comprises a gate oxide 1110/1120 on the substrate and a gate conductive layer 1350/1356/1160/1170. The difference between Ito and the claimed invention is spacers on the sides of the gate and a fourth lightly doped region of the second type adjacent to the first doped region and beneath one of the spacers. Figure 1B of McElheny discloses a MOSFET with sidewall spacers and light doped regions beneath the spacers (LDD structure). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Ito by including sidewall spacers and a fourth lightly doped region (LDD structure). The ordinary artisan would have been motivated to modify Ito in the manner described above for the purpose of further isolating the gate to prevent build-up of device capacitance (col. 1, lines 44-47 of McElheny) and further suppressing hot carrier generation, which is well known in the art. This rejection similarly applies to claims 11, 12, 25 and 26.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas

TOM THOMAS
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TECHNOLOGY CENTER 2800

Matthew C. Landau

Examiner

September 12, 2004